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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/693,976	10/28/2003	Su Tao	TAOS3012/EM	5780

23364 7590 04/27/2005

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EXAMINER	
IM, JUNGHWA M	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 04/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

4A

Office Action Summary	Application No.	Applicant(s)	
	10/693,976	TAO ET AL.	
	Examiner	Art Unit	
	Junghwa M. Im	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election with traverse of Embodiment 1 in the reply filed on February 9, 2005 is acknowledged. The traversal is on the ground(s) that the office has not demonstrated why the species shown are not considered to be distinct. In particular, Applicant argues that "All embodiments share the thermal layer 4, chips 3, a, and the substrate, differing only in the connection means (adhesive vs. 'bumps')." This is not found persuasive. First of all, each of five embodiments in the instant invention has a distinctive configuration in the heat spreader. Furthermore, each embodiment has a different way of stacking/arranging the chips while applying a different manner of the electrical connection to the substrate. Additionally, it is pointed out that Embodiment 1 reads on claims 1-12.

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 5 recites a limitation of "the substrate further comprises a grounding layer." It is pointed out that the instant invention merely discloses that the substrate has a circuit layer.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 7, 10 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Sherif et al. (US 5724729), hereinafter Sherif.

Regarding claim 1, Fig. 4 of Sherif shows a thermal enhance MCM package, comprising:

a first chip [41] having a first active surface and a first bonding pad formed on the first active surface;

a second chip [46] having a second active surface and a second bonding pad formed on the second active surface;

a substrate [10] having an upper surface with a first mounting area, a second mounting area and a contacting area, wherein the first chip and the second chip are disposed on the first mounting area and the second mounting area respectively and are electrically connected to the substrate [through the balls 22]; and

a thermally conductive device [35] disposed on the contacting area [the end portions attached by the adhesive 28] and covering the first chip and the second chip.

Regarding claim 2, Fig. 4 of Sherif shows the thermally conductive device comprises a first chip connecting portion [a portion attached by 51] connecting the first chip, a second chip connecting portion [a portion attached by 55] connecting the second chip, a substrate connecting portion [end portions attached by 28] connecting the substrate, and a joint portion [top edges of

the heat spreader 35] connecting the substrate connecting portion, the first chip connecting portion and the second chip connecting portion with each other, and the substrate connecting portion is attached to the contacting area.

Regarding claim 3, Fig. 4 of Sherif shows a thermally conductive adhesive [28; solder] attaching the thermally conductive device to the substrate.

Regarding claim 7, Fig. 4 of Sherif shows the first chip and the second chip are bonded and electrically connected to the substrate via bumps [22].

Regarding claim 10, Fig. 4 of Sherif shows the thermally conductive device is a heat spreader (col. 6, line 67).

Regarding claim 12, Fig. 4 of Sherif shows a plurality of solder balls [12] formed on a lower surface of the substrate (col. 6, lines 25-26).

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Takahashi et al. (US 6351194), hereinafter Takahashi.

Regarding claim 1, Fig. 7 of Takahshi shows a thermal enhance MCM package, comprising:

a first chip [13a] having a first active surface and a first bonding pad formed on the first active surface;

a second chip [13b] having a second active surface and a second bonding pad formed on the second active surface;

a substrate [11] having an upper surface with a first mounting area, a second mounting area and a contacting area [an area contacting a portion 71], wherein the first chip and the second chip are disposed on the first mounting area and the second mounting area respectively and are electrically connected to the substrate [through the balls 13x]; and

a thermally conductive device [71] disposed on the contacting area and covering the first chip and the second chip.

Regarding claim 11, Fig. 7 of Takahshi shows a material of the thermally conductive device comprises copper (col. 4, lines 28-31).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sherif in view of Huang et al. (US 6703698), hereinafter Huang.

Regarding claim 4, Fig. 4 of Sherif shows most aspect of the instant invention including the substrate further comprises a circuits layer (col. 6, lines 6-8), however, fails to show that the substrate comprises "a via formed on the contacting area, and the via is filled with a thermally conductive adhesive and connected to the circuits layer." Fig. 2E of Huang shows a thermal enhanced semiconductor package wherein the substrate comprises a circuit layer (power, ground,

I/O), a via (210a, 210b, 210c) formed on the contacting area, and the via is filled with a thermally conductive adhesive and connected to the circuits layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Huang into the device of Sherif in order to have the substrate comprising a circuit layer, a via formed on the contacting area, and the via is filled with a thermally conductive adhesive and connected to the circuits layer to enhance the electrical performance.

Regarding claim 5, Fig. 4 of Sherif shows most aspect of the instant invention except "the substrate further comprises a grounding layer, a via formed on the contacting area, and an electrically conductive layer is formed on an inner wall of the via and electrically connected to the grounding layer." Fig. 2E of Huang shows a thermal enhanced semiconductor package wherein the substrate comprises a ground layer, a via (210b) formed on the contacting area, and the via is filled with a thermally conductive adhesive and connected to the circuits layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Huang into the device of Sherif in order to have the substrate comprising a ground layer, a via formed on the contacting area, and the via is filled with a thermally conductive adhesive and connected to the ground layer to enhance the ground effect.

Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sherif in view of Akram (US 6703698).

Regarding claims 8 and 9, Fig. 4 of Sherif shows most aspect of the instant invention

except an underfill disposed between the first chip/the second chip and the substrate. Fig. 3 of Akram shows a thermal enhanced semiconductor package wherein an underfill [44] disposed between the first chip/the second chip [20's] and the substrate [12].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Akram into the device of Sherif in order to have an underfill disposed between the first chip/the second chip and the substrate to protect the connecting bumps under the chips.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sherif and Huang as applied to claim 5 above, and further in view of Hashemi (US 6611055).

Regarding claim 6, the combined teachings of Sherif and Huang show most aspect of the instant invention except "the electrically conductive layer is a copper layer." Hashemi discloses a thermal enhanced semiconductor package with an electrically conductive layer of the via is a copper layer (col. 5, lines 39-42).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Hashemi into the device of Sherif and Huang in order to have an electrically conductive layer of the via made of a copper layer for an better conductivity.

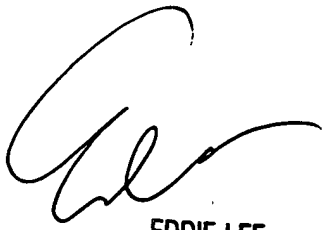
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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